VDU-B

Function.

This board generates the characters by converting ASCII data to a dot pattern which is combined with the video sync. signals from board A and provides a composite video signal. Options are available to either flash characters or to invert them from white on black to black on white.

Operation.

Line and field syncs are mixed in half of IC15 to give MS, and combined with the video information in IC12. Line blanking (LBLNK) is ginerated using parts of IC14 & 3a, so that no characters can be displayed in either margin. Similarly, a frame blanking signal (FBLNK) is produced by parts of IC14 & 15 to suppress characters in the top and bottom margins. The input B may be used to make characters flash. The blanking signals are all combined by IC13 to give the video blanking signal (BVID).

ASCII data is applied to the character generator ROM (IC6) and the dot pattern appears at the outputs. These outputs are turned into a serial dot sequence by the shift register IC5. Timing signals for loading the shift register and latching the ASCII data on the G Board are generated by the decoder IC4 driven by a counter IC8. This counter is incremented by the dot clock and synchronised by LSD. With L2 open circuit the counter functions in its normal role as a divide by ten counter. But with L2 closed the counter is reset by the decoder and becomes a divide by nine counter. This has the effect of reducing the gap between characters.

Depending on the position of L1 the output from the shift register may be fed either direct to the video output or via IC9. DV7 may be used either to control IC9 and invert the video image from white characters on a black background to black on white, or to control IC1 & IC7 and cause characters to flash.

The board is arranged to provide a standard 1V p-p video output and to accommodate a UHF modulator to allow direct connection to a TV. IC2 can be used to reduce flicker on the screen when the MPU is accessing the video RAM by blanking the picture. This can be omitted if necessary.

Options and Notes.

1. UHF output not required.

   Omit R3-R9, C1, C9, T1 and the UHF modulator.

2. Video output not required.

   Omit R10-R12, D1, C5-6.

3. Video inversion not required.

   Omit IC9 and fit L1 in the shorter position.

4. Flashing characters not required.

   Omit IC1, R1-2, C3 and omit link B-B.

5. For reduced gap between characters fit L2; otherwise leave it out.

6. For single-supply character generators (e.g. RO3-2513) omit D3, R19.

7. The board is laid out to link D7 into the video inversion circuitry, and a piece of insulated wire should be used to link D7 to IC7 if the flashing option is required instead. A switch can be used to change between these options by fitting pull-down resistors of 1K (3K3 for 'LS) to pin 12 IC9 and pin 1 IC7 and switching DV7 to either pin. Don't forget to link B-B when using the flash option.

8. When either option is omitted and inputs 9 & 10 of IC13 are not used, the inputs can be left open circuit to float high or connected to +5V.

9. R6 can be either a fixed resistor as specified or a 4K7 preset to allow the video level to be adjusted. When using a preset, replace the link adjacent to R10 by a 1K resistor.

JSD 10.12.78.

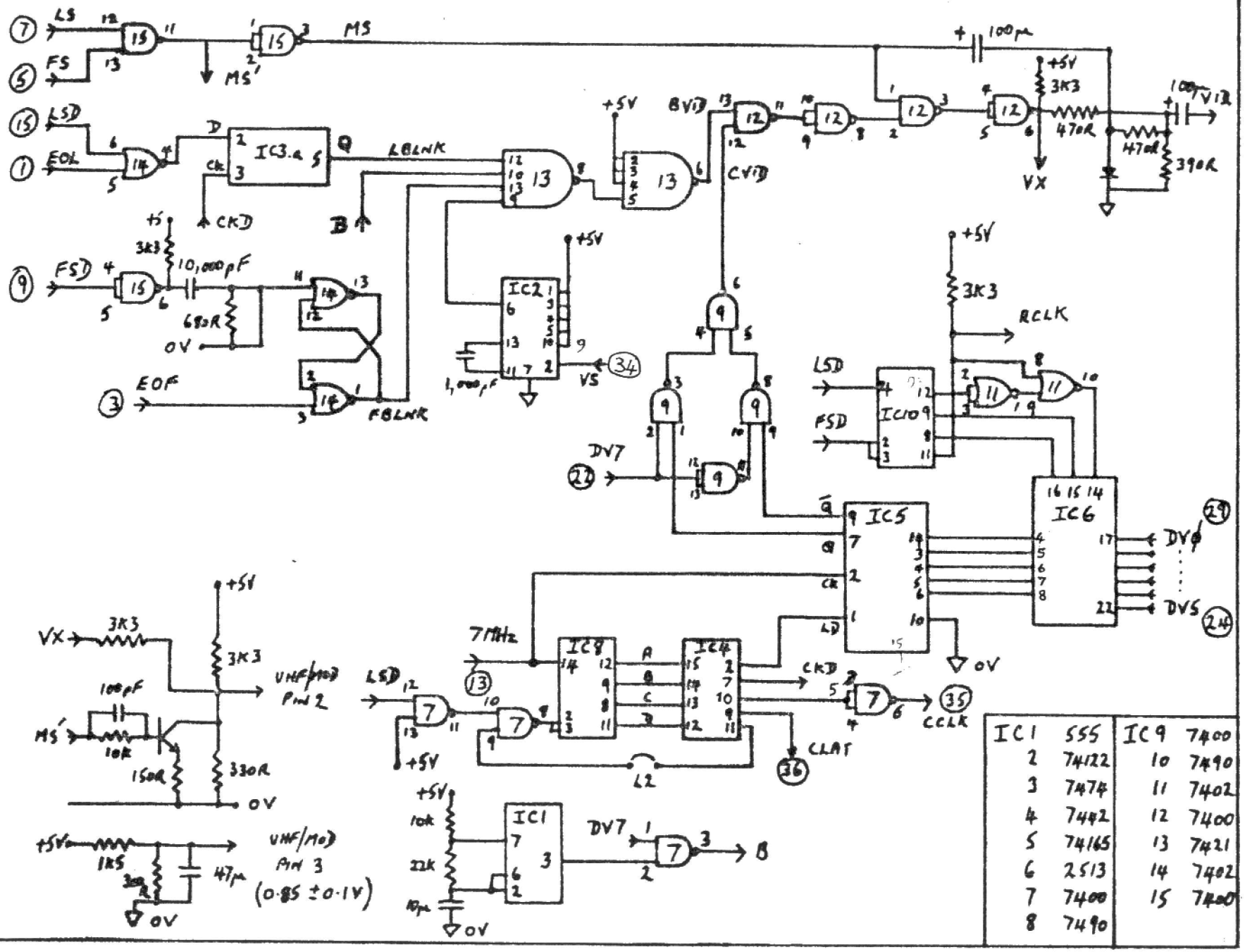
Kemitron Electronics

VDU.B.7

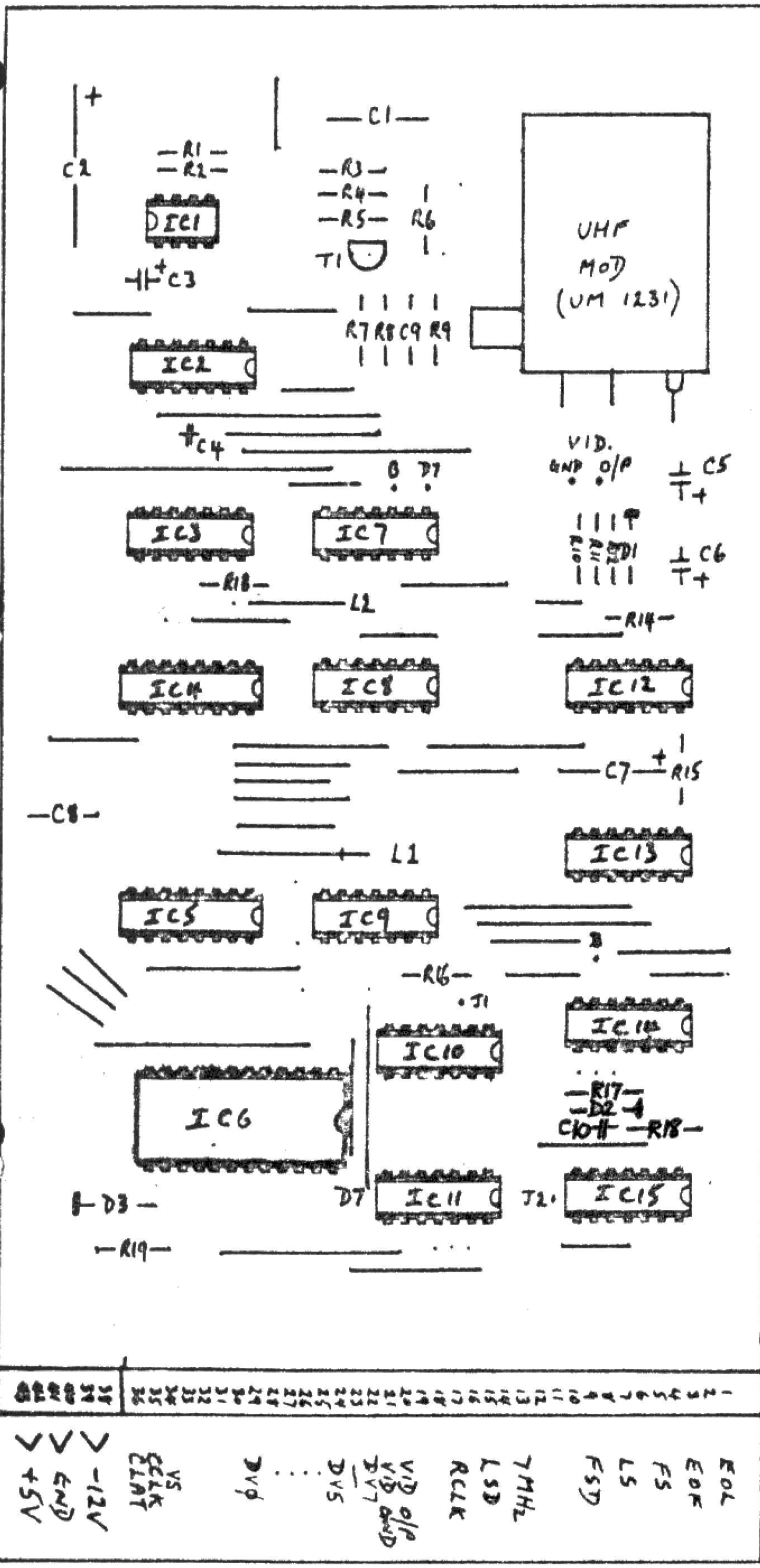
Drn. TSD

Date 6/12/78

Revn A 17-11-79



IC1	555	IC9	7400
2	74122	10	7490
3	7474	11	7402
4	7442	12	7400
5	74165	13	7421
6	2513	14	7402
7	7400	15	7400
8	7490		



COMPONENTS

C1	47µ 10V		
2	100µ 10V		
3	10µ 10V TANT		
4	1,000 pF		
5	100µ 10V		
6	100µ 10V		
7	47µ 10V		
8	0·1µ DISC		
9	100 pF		
10	10,000 pF (2,200 pF)		
R 1	10K	11	390R
2	22K	12	470R
3	300R, 2%	13	3K3 (10K)
4	330R	14	3K3
5	150R	15	10R
6	3K3	16	3K3 (10K)
7	1K5	17	680R ([illegible])
8	10K	18	3K3 (10K)
9	3K3	19	470R
10	470R		

D1, 2	1N914
D3	5V1 BZY88
T1	2N3704

IC1	555
2	74122
3	7474
4	7442
5	74165
6	2513
7	7400
8	7490
9	7400
10	7490
11	7402
12	7400
13	7421
14	7402
15	7400

'LS SERIES DEVICES CAN BE USED, EXCEPT FOR IC12. IF 'LS USED, CHANGE RESISTORS TO BRACKETED VALUES.

Kemitron Electronics

VDU·B·7

Drn. J.S.D | Date 5/12/78